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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,476	01/15/2004	Seong-Hak Moon	P-0642	4149

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FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER	
BODDIE, WILLIAM	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,476	MOON, SEONG-HAK	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☒ Claim(s) 9 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 1/15/04 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 5/17/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: page 7 line 8 currently reads: "At this time, the scan driving IC 145 is includes..." This is incorrect grammatically. Also on page 7, in line 14, the lower voltage generating unit and the amplifying unit are labeled inconsistently with the rest of the disclosure. The lower voltage generating unit is labeled as 320, while the amplifying unit is labeled as 330. The problem arises once more on page 7, line 25.

Appropriate correction is required.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the amplifying unit comprising a transistor connected to the output of the OP-AMP must be shown or the feature(s) canceled from claim 5. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 9 is objected to because of the following informalities: the claim currently reads, "the switching devices comprises a FET." This is incorrect grammatically. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 12 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, claim 12 requires that the lower voltage generating unit be operated on the basis of the upper switching control signal. There is no mention of this with the drawings or specification. It appears that the Applicant intended the claim to instead require that the lower voltage generating unit be controlled by a lower switching control

signal. For the purposes of this office action the following discussion of claim 12, will be with this assumption in mind.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kanazawa (US 5,420,602).

With respect to claim 1, Kanazawa discloses, an apparatus (fig. 27) for driving a flat display panel (PDP in fig. 27) comprising a scan driving unit (D_3 and 105 in fig. 40) for controlling an upper voltage value (Va controlled by D_3) and a lower voltage value (Vs controlled by 105) which are applied to an IC (104 in fig. 40) for driving a scan electrode of a flat display panel.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa (US 5,420,602) in view of Furuhashi et al. (US 6,756,958).

With respect to claim 2, Kanazawa discloses, the apparatus of claim 1 (see above).

Kanazawa does not expressly disclose, an amplifying unit.

Furuhashi discloses, control circuitry to generate currents and voltages, wherein a scan driving unit (104, 105 in fig. 1) further comprises an amplifying unit (312-314 in fig. 2) for amplifying an upper voltage value to a predetermined level (col. 4, lines 18-31).

Furuhashi and Kanazawa are analogous art because they are both from the same field of endeavor namely design of the control circuitry of a scan driver for a flat display panel.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the amplifying circuitry, taught by Furuhashi, in the upper voltage generating means of Kanazawa.

The motivation for doing so would have been to increase picture quality (Furuhashi; col. 2, lines 16-21).

Therefore it would have been obvious to combine Kanazawa with Furuhashi for the benefit of enhanced display quality to obtain the invention as specified in claim 2.

With respect to claim 3, Kanazawa and Furuhashi disclose, the apparatus of claim 2 (see above).

Furuhashi further discloses, wherein the amplifying unit comprises an OP-AMP (col. 4, lines 17-23).

With respect to claim 4, Kanazawa discloses, the apparatus of claim 1 (see above).

Kanazawa does not expressly disclose, an amplifying unit.

Furuhashi discloses, control circuitry to generate currents and voltages, wherein a scan driving unit (104, 105 in fig. 1) further comprises an amplifying unit (312-314 in fig. 2) for converting an upper voltage value to a current and amplifying the converted current to a predetermined level (col. 4, lines 18-31).

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the amplifying circuitry, taught by Furuhashi, in the upper voltage generating means of Kanazawa.

The motivation for doing so would have been to increase picture quality (Furuhashi; col. 2, lines 16-21).

Therefore it would have been obvious to combine Kanazawa with Furuhashi for the benefit of enhanced display quality to obtain the invention as specified in claim 2.

With respect to claim 5, Kanazawa and Furuhashi disclose, the apparatus of claim 4 (see above).

Furuhashi further discloses, wherein the amplifying unit comprises an OP-AMP (313 in fig. 2; col. 4, lines 17-23) and a TR (314 in fig. 2; col. 4, lines 19-23) connected to an output terminal of the OP-AMP (clear from fig. 2).

10. Claims 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa (US 5,420,602) in view of Moon (US 2002/0196210).

With respect to claim 6, Kanazawa discloses, the apparatus of claim 1 (see above), wherein the scan driving unit comprises:

an upper voltage generating unit (D_3 in fig. 40); and

a lower voltage generating unit (105) for outputting a lower voltage value on the basis of a lower switching control signal (Y-UD, Y-DD in fig. 40).

Kanazawa does not expressly disclose that the upper voltage generation is controlled by an upper switching control signal.

Moon discloses, an upper voltage generating unit (510 in fig. 6) for outputting an upper voltage value on the basis of an upper switching control signal (first and second reset data in fig. 6).

Moon and Kanazawa are analogous art because they are both from the same field of endeavor namely, design of the control circuitry of a scan driver for a flat display panel.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the diode of Kanazawa with the upper voltage generating unit of Moon.

The motivation for doing so would have been to reduce power consumption and extend the durability of the electrodes (Moon; para. 39).

Therefore it would have been obvious to one of ordinary skill in the art to combine Kanazawa with Moon for the benefit of reduced power consumption to obtain the invention as specified in claim 6.

With respect to claim 7, Kanazawa and Moon disclose, the apparatus of claim 6 (see above).

Kanazawa further discloses, wherein the scan driving unit selectively outputs one of the outputted upper voltage value (Vy in fig. 40) and the outputted lower voltage value (output of 105' in fig. 40), on the basis of a timing control signal (Y-STB2, Y-STB1, Q1 in fig. 40).

With respect to claim 8, Kanazawa and Moon disclose, the apparatus of claim 7 (see above).

Kanazawa further discloses, switching devices having a push-pull form (T1 and T2 in fig. 40) turned on/off on the basis of the timing control signal (clear from fig. 40).

With respect to claim 9, Kanazawa and Moon disclose, the apparatus of claim 8 (see above).

Kanazawa further discloses, wherein the switching devices comprises a FET (T1 and T2 in fig. 40; col. 24, lines 37-41).

With respect to claim 10, Kanazawa and Moon disclose, the apparatus of claim 6 (see above).

Moon further discloses, wherein the upper voltage generating unit comprises switching devices (SW4, SW5 in fig. 10) having a push-pull form turned on/off on the basis of the upper switching control signal (para. 129).

With respect to claim 11, Kanazawa and Moon disclose, the apparatus of claim 10 (see above).

Moon further discloses, wherein the switching devices comprise a FET (para. 129).

With respect to claim 12, Kanazawa and Moon disclose, the apparatus of claim 6 (see above), wherein the lower voltage generating unit (105 in fig. 40) comprises switching devices (T3 and T4 in fig. 40) having a push-pull form (clear from fig. 40) turned on/off on the basis of the lower switching control signal (Y-UD, Y-DD in fig. 40).

With respect to claim 13, Kanazawa and Moon disclose, the apparatus of claim 12 (see above), wherein the switching devices comprise a FET (T3 and T4 in fig. 40; note the symbols used for the transistors; also see col. 24, lines 51-56).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (US 6,281,633) discloses control circuitry for a plasma display panel with upper and lower voltage waveform generators. Yanagi et al. (us 5,929,847) discloses, voltage generating circuitry, specifically note figure 10.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Wlb
9/12/06

AMR A. AWAD
SUPERVISORY PATENT EXAMINER